

**CLAIMS**

Amend the claims as follows.

1. (Canceled)
2. (Canceled)
3. (Canceled)
4. (Canceled)
5. (Canceled)
6. (Canceled)
7. (Canceled)
8. (Currently amended) A circuit comprising:  
a data input terminal;  
a pull-up circuit and a pull-down circuit coupled to the data input terminal; and  
a data node formed at a junction of the pull-up circuit and the pull-down circuit;  
~~a pass transistor coupled between the data node and a data pad; and~~  
~~a driving circuit structured to drive the pass transistor;~~  
wherein the pass transistor is operative when the circuit is in a data input mode and in  
a data output mode; and  
wherein the pull-up circuit is structured to be driven by a static voltage.
9. (Original) The circuit of claim 8 wherein the pull-up circuit comprises first  
and second serially coupled transistors.
10. (Original) The circuit of claim 9 wherein the first transistor is structured to be  
driven by a transistor driving circuit coupled to the data input terminal.

AMENDMENT

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11. (Currently amended) A The circuit of claim 10, comprising:  
a data input terminal;  
a pull-up circuit and a pull-down circuit coupled to the data input terminal;  
a data node formed at a junction of the pull-up circuit and the pull-down circuit;  
a pass transistor coupled between the data node and a data pad; and  
a driving circuit structured to drive the pass transistor;  
wherein the pass transistor is operative when the circuit is in a data input mode and in  
a data output mode;  
wherein the pull-up circuit comprises first and second serially coupled transistors;  
wherein the first transistor is structured to be driven by a transistor driving circuit  
coupled to the data input terminal; and  
wherein the second transistor is structured to be driven by a static voltage.

12. (Original) The circuit of claim 11 wherein the data input terminal is coupled to a circuit core, and wherein the static voltage is a power supply voltage of the circuit core.

13. (Currently amended) The device of claim 8 wherein the driving circuit comprises:  
a first voltage input to receive a first power supply voltage;  
a second voltage input to receive a second power supply voltage, the second power supply voltage higher than the first power supply voltage;  
an input terminal structured to receive a voltage level signal from the a data pad;  
a voltage sensor coupled to the input terminal and structured to generate a control signal based on the voltage level of the data pad;  
a control circuit coupled to the voltage sensor and structured to generate an output signal responsive to the control signal.

14. (Original) The device of claim 13 wherein the control circuit is coupled to the first voltage input and to the second voltage input, the control circuit structured to generate the output signal from the first power supply voltage or from the second power supply voltage, responsive to the control signal.

15. (Original) The device of claim 14 wherein, when the pad voltage is above a threshold voltage, the control circuit generates the output signal from the first power supply voltage.

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Currently amended) A ~~The method of claim 20, comprising:~~  
sensing a voltage at a data pad;  
when the sensed voltage is below a threshold value, driving a pass transistor coupled  
to the data pad with a first driving signal; and  
when the sensed voltage is above the threshold value, driving the pass transistor with  
a second driving signal;

wherein driving a pass transistor with a first driving signal comprises driving a pass transistor with a static voltage having a first value.

22. (Original) The method of claim 21 wherein driving a pass transistor with a second driving signal comprises driving a pass transistor with a static voltage having a second voltage value, the second voltage value less than the first voltage value.

23. (Original) The method of claim 22 wherein the second voltage value is a value between a power supply voltage of a device that generated a data signal at the data pad and a power supply voltage of a device that is using the data signal from the data pad.

24. (Currently amended) The method of claim 20 21 further comprising, before sensing a voltage at a data pad, driving a data signal to the data pad.

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (New) The circuit of claim 8 comprising:  
a pass transistor coupled between the data node and a data pad; and  
a driving circuit structured to drive the pass transistor.